Module and Application Description

PROCONTROL P

Analog Control

Control Module

For Analog Control Functions with Continuous Output, 1- and 2-fold

1KGD 003 930, Edition 08/05

83SR07-E/R1210

Application

The module is used for stored-program analog control of one or two process variables. The module is provided with two continuous outputs for output of the correcting variables. The following types of actuators can be controlled:

- electrohydraulic actuators
- electropneumatic actuators
- electric-motor-powered drives

The drives are positioned either locally at the transducer or in case of electric-motor-powered actuators, in a continuously operating power electronics system. It is also possible to supplement the single variable analog controls by a higher-level master control system.

The module is intended for use in connection with the process operator station.

The module incorporates the function blocks for implementing continuous single variable controllers. Additional function blocks are available for signal conditioning.

In the analog control mode, the module is used with fixed cycle times. This is 100 ms for one actuator and 200 ms for two actuators.

The cycle time is specified by means of function block KON, which is the first block to appear in the structure.

The module incorporates two hardware process interfaces for the power controller units and the process.

Features

The module address is set automatically by plugging the module into the PROCONTROL station.

The telegrams received via the bus are checked by the module for error-free transfer by means of their parity bits.

The telegrams sent by the module to the bus are provided with parity bits to ensure error-free transfer.

The user program is stored in a non-volatile memory (EEPROM). It can be loaded and changed from the PDDS via the bus.

The module is ready for operation as soon as a valid user list is loaded.

For communication with the process and the switchgear, the module requires the following voltage:

USA/USB operating voltage +24 V

internally branched into the voltages:

UK1	supply of contacts of process interface 1
UK2	supply of contacts of process interface 2
S11/S13	supply of transducer of process interface 1
S21/S23	supply of transducer of process interface 2

These voltages are short-circuit-proof and designed to prevent any interaction.

The operating voltages and the external logic signals are related to reference conductor Z.

The following annunciations are indicated on the front panel of the module by LEDs:

ST	disturbance
SG	module disturbance

The LED ST signals any disturbance in the module and in data communication with the module.

The LED SG signals module disturbances only.

Module design

The module comprises:

- Process interfaces
- Station bus interface
- Processing section

Process interface

In the process interfaces the process signals are adapted to the internal signal level of the module.

Station bus interface

In the station bus interface the module signals are adapted to the bus. This essentially involves a parallel/serial conversion.

Processing section

In order to process the signals coming from the process and the bus, the module is provided with a microprocessor which co-operates with the following memory areas via an internal bus of the module:

Contents	Storage medium
Operating program	EPROM
Function blocks	EPROM
User program (structure, address, parameters, limit value and simulation list)	EEPROM
User program (structure, address, parameter, limit value and simulation list)	RAM
History values	RAM
Current module input and output signals (shared memory)	RAM

The operating program enables the microprocessor to perform the operations of the module.

The function block memory contains the software modules needed to implement the various functions.

All function blocks together with their inputs and outputs can be called by the user via the Programming, Diagnostic and Display System (PDDS).

The user program memory contains the following information:

- how the function blocks are interconnected,
- which module inputs and outputs are allocated to the inputs and outputs of the function blocks,
- which constants are specified to the individual inputs of the function blocks,
- which parameters are specified to the individual inputs of the function blocks,
- which plant signals are allocated to the module inputs and outputs,
- which function blocks serve the process interfaces,
- which limit values are allocated to the analog values,
- which calculated function results, module input and output signals are simulated.

This information is specified by the user according to the plant involved.

The complete user program is filed in an EEPROM for normal operation. For optimizing purposes, it is possible to work with a modified copy of the user program in RAM, which must be taken over into the EEPROM upon completion of optimization.

Settings can be either preset by the user directly at the appropriate function block inputs or specified in a separate parameter list.

When limit signals are generated by means of function block GRE, the limit values (4 per GRE) are specified in a limit values list.

Parameter and limit value lists can be changed (on-line) at anytime during operation. In this case they are stored in the RAM or EEPROM, depending on whether they are assigned to the RAM or EEPROM mode.

Data exchange of the module with the bus system is performed via the memory for the module input and output signals. It buffers the signals.

Structuring

During structuring module inputs and outputs are allocated to the neutral inputs and outputs of the function blocks or constants and parameters or output from other function blocks (calculated function results) are specified to the function block inputs. Structuring is performed on the basis of data supplied by the user in the form of a so-called structure list.

The following limit values of the module shall be observed for structuring:

- max. number of module inputs 287
- max. number of simulated calculated function results, module inputs and outputs 32
- max. number of module outputs 223
- max. number of calculated function results 255
- max. number of timers 136
- max. number of parameters 80
- max. number of limit value sets 16
- max. number of drive control functions ASP 2
- max. number of lines in the structure list 2823
- length of historic values list (bytes) 1024
- design of shared memory (see “Addressing”)

A line is an entry on the PDDS.

For the precise procedure of structuring the function blocks, please refer to the respective function block descriptions.

Addressing

General

The signal exchange between the module and the bus system is performed via a shared memory. Incoming telegrams to be received by the module and calculated function results intended to leave the module are buffered in the shared memory.

The shared memory has send registers for telegrams to be transmitted and receive registers for telegrams to be received. The register numbers 0 to 63 are defined as send registers and the register numbers 64 to 199 as receive registers.

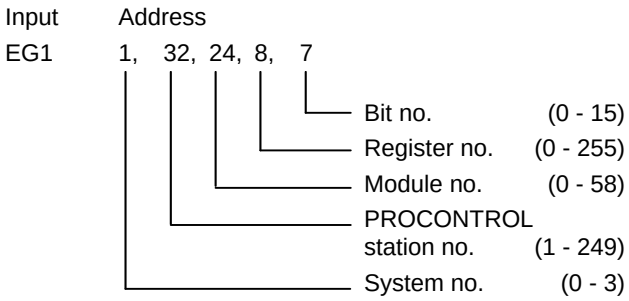
The module input and output signals are allocated to the shared memory registers as specified by the user via the PDDS.

The user data are contained in address lists.

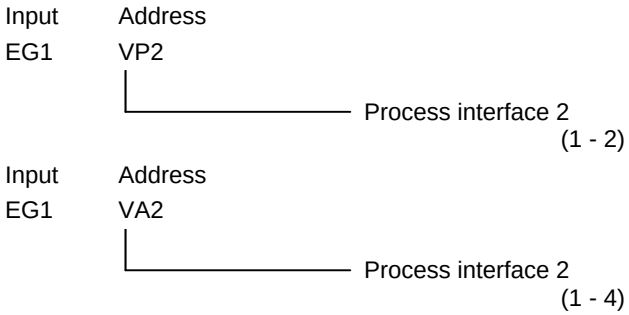
Address list for module inputs

In the address list for module inputs, each module input is assigned the send-location address or the process interface of the signal to be received.

In the case of module inputs that receive their signals over the bus, addressing is done by allocating the send-location address to EGn, e.g.:



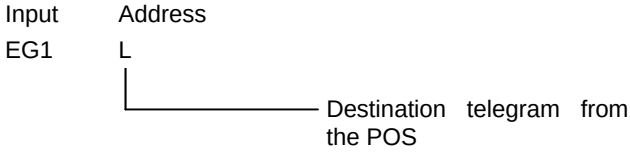
In the case of module inputs that receive their signals via the process interface, addressing is done by allocating the process interface to EGn. In this case, a distinction is to be made between contact inputs (VPn) and analog inputs (VAn), e.g.:



VAn allocation:

VA1:	Analog input	E11 of	process interface	1
VA2:	Analog input	E21 of	process interface	2
VA3:	Analog input	E13 of	process interface	1
VA4:	Analog input	E23 of	process interface	2

In the case of module inputs which receive their signal from the process operator station (POS), addressing is done by allocating L to EGn, e.g.:



The address list for inputs is translated by the PDDS into two internal lists, the “Bus address list“ and the “Module inputs allocation list“.

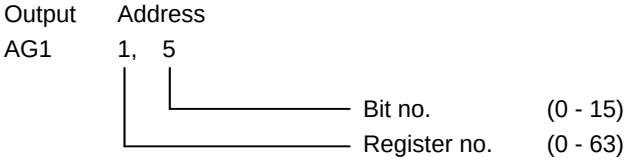
The bus address list contains, for all the telegrams to be used by the module, the send-location address and the receive register number.

Telegrams received, whose addresses are contained in the bus address list, are registered in the receive register of the shared memory. Telegrams received, whose addresses are not contained in the bus address list, are ignored by the module.

The "Module inputs allocation list" contains the associated receive register number for each module input and, in the case of binary values, the bit position.

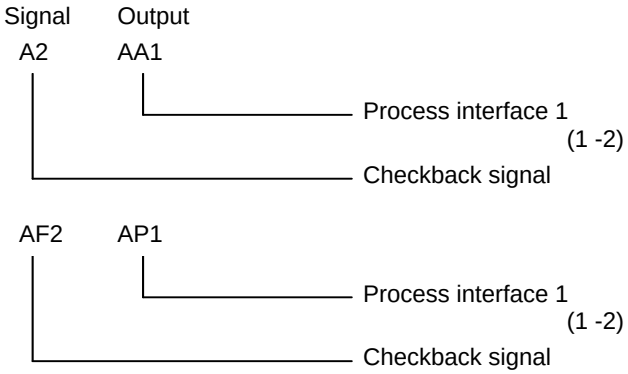
Address list for module outputs to the bus

In the address list for module outputs, a send register is defined for every signal which is to leave the module, and in the case of binary signals, a send bit is defined in addition, e.g.:



Addressing of the process interface for the outputs

In the case of module outputs that issue their signal to the process interface, addressing is done in the structure list by allocating AAn (analog outputs) and APn (drive releases), n being the number of the process interface, e.g.:



Address formation

System address and station address are set at the station bus coupling module or at the station-bus control module and are transferred by that module to all the modules of the relevant PROCONTROL station.

The module addresses are defined through the connections on the backplane so that the modules are adjusted automatically when being plugged into a slot.

Limit value list

The limit value list contains 4 limit values, each for a maximum of 16 GRE function blocks (limit signal generation for an analog value). The list is stored in the EEPROM and — for RAM mode — in the RAM.

The PDDS can always be used to change the limit value list via a “job memory“ (RAM). Such changes are stored in the EEPROM in the case of EEPROM mode, or in the RAM in RAM mode.

When the user lists are transferred from the RAM to the EEPROM, and vice versa, the limit value list is transferred as well.

Parameter list

The parameter list contains up to 80 values for parameters of the function blocks. It is handled and saved like the limit value list.

Simulation list

The PDDS can be used to overwrite and "simulate" a maximum of 32 module signals (function results, module inputs and module outputs). This simulation list is handled and saved like the limit value list.

Event generation

For each system cycle, the module is prompted once by the PROCONTROL system to send the data stored in the send registers of the shared memory.

If values change, this fact is treated like an event.

The module recognizes the following conditions as an event:

- Change of a binary value
- Change of an analog value by a fixed threshold of 0.39 % and expiration of a timeout of 200 msec since the last transmission (cyclically or per event).

As soon as an event occurs, the cyclic mode is interrupted and the new values are given priority and transmitted to the bus.

Disturbance bit evaluation, receive monitoring function

The telegrams received over the bus may have a fault flag set in bit position 0. The fault flag is generated by the sending module based on plausibility checks and is set to "1" if specific disturbances occur (cf. the relevant module or function block descriptions).

In order to be able to recognize errors in signal transfer, the module includes a feature that monitors the input telegrams for cyclic renewal. If a signal has not been updated for a particular period of time (e.g. on account of a failure of the sending module), the bit of position 0 in the assigned receive register of the shared memory will be set to "1". At the same time, all binary values are set to "0" in binary value telegrams. In the case of analog values, the previous value is retained.

A set disturbance bit does not automatically trigger a reaction in the module. If the disturbance bit of a telegram is to be evaluated, this must be taken into consideration when structuring.

The disturbance bits of received telegrams can only be used internally. They are not included in telegrams to be sent.

Diagnosis and annunciation functions

Disturbance annunciations on the module

The following annunciations are signalled on the front panel of the module:

	Designation of LED
- Disturbance	ST
- Module disturbance	SG

The LED ST annunciates all disturbances in the module and disturbances in data communication with the module.

The LED SG annunciates module disturbances only.

Disturbances of the process interface

Monitoring is limited to structured process inputs and outputs.

Disturbances are signalled by the light-emitting diode ST and by the diagnostic register message 'process channel fault'. In addition, the disturbance bit is set in the appropriate receive register.

Disturbance signals to the annunciation system

The alarm annunciation system and/or the control diagnosis system CDS receive disturbance messages from the control module via the bus.

Diagnosis

The incoming telegrams, the generation of the telegrams to be transmitted, and internal signal processing are monitored for errors in the processing section of the module (self-diagnosis).

If a disturbance occurs the type of disturbance is filed in the diagnosis register and, at the same time, a disturbance signal is transmitted to the PROCONTROL system.

When requested, the module transmits a telegram containing the data stored in the diagnosis register (register 246) (see Fig. 1).

Fig. 1 shows the contents of the diagnosis register, the signals of the general disturbance lines, the annunciations on the CDS, and the ST and SG annunciations.

If the annunciation 'process channel fault' appears in the diagnosis register this may be due to any of the following causes:

- Short-circuit at the outputs UK1, UK2, AF1, AF2, S11/S13 or S21/S23.
- Analog input values not plausible, i.e. the values are smaller than - 6.25 % or bigger than 150 %.
- Open circuit at the analog outputs AY1 or AY2 in the configuration 4 ... 20 mA.

If the annunciation 'processing fault' appears in the diagnosis register, this may be due to any of the following causes:

- Invalid structuring
- Relay driver for the analog inputs or outputs of function unit 1 (E11/E12, E13/E14, AY1) or function unit 2 (E21/E22, E23/E24, AY2) defective.
- Analog section for analog output AY1 or AY2 defective.
- Internal module voltages disturbed.
- Internal reference values of the analog inputs and outputs-disturbed.

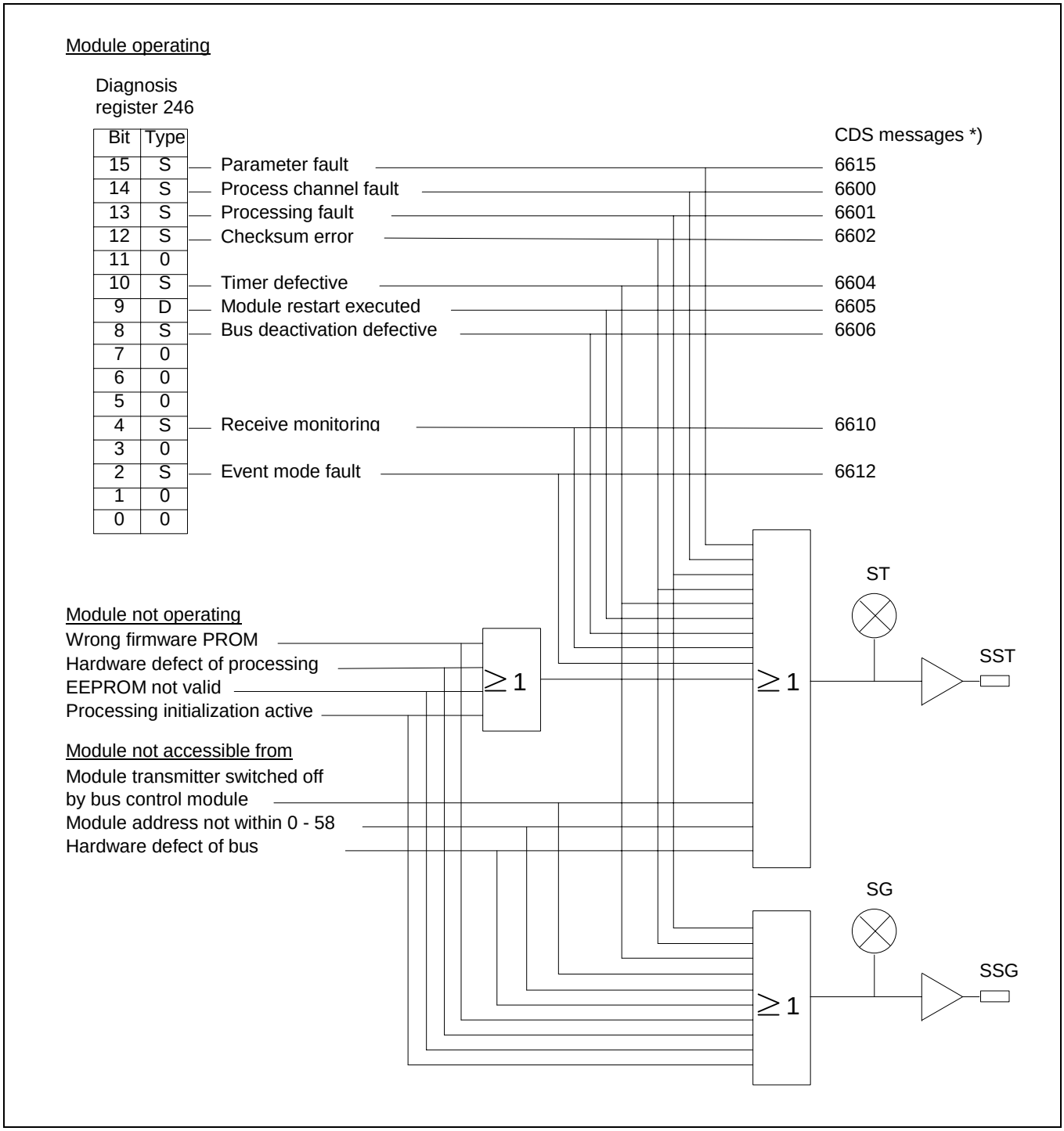


Fig. 1: 83SR07 diagnosis messages

*) The control diagnosis system (CDS) provides a description for every annunciation number. The description provides, among other data:

- Information on cause and effect of the disturbance
- Recommendations for its elimination.

This makes for fast elimination of disturbances.

Operating states of the module

Initialization and bootstrapping with user lists

Initialization is accomplished either by plugging the module into its slot or after connection of the voltage.

The initialization process causes the module to assume a defined initial state. The light-emitting diodes ST and SG light during initialization.

No user program is available when the module is started up for the first time. The module signals “Processing fault” and the disturbance LEDs ST and SG are activated.

As a first step, it is necessary to transfer the user program from the PDDS via the bus to the RAM of the module. If this operation is started with the structure list, the PDDS will call all the other lists automatically. To avoid the transmission of incorrect lists, the PDDS checks the place of installation and the address before each transmission job. The module checks each incoming list for plausibility.

Now, the complete user program can be transferred to the EEPROM by command from the PDDS.

Following this, the module is ready for operation, and the LEDs ST and SG are deenergized.

Normal operation

The module processes the user program stored on the EEPROM.

In normal operation, the signals received via the bus and the process interfaces are processed in accordance with the instructions contained in the structure list.

In line with these instructions, commands are output to the power unit, and checkback signals indicating the process status are transmitted via the bus..

Modifying the parameter and limit value lists

The parameters and limit values can be changed from the PDDS (see ”Limit value list” and ”Parameter list”).

Modifying the structure and address lists

The structure and address lists can be transferred to the PDDS, modified, and retransferred to the module. The following procedure should be followed:

- The module should be in the EEPROM mode
- Copy the list to be modified from the EEPROM (or RAM) to the PDDS and modify list
- Retransfer the modified list into the RAM of the module.
- Switch the module from EEPROM mode to RAM mode, using the PDDS command ”UMS” and test new lists.
- Switch to EEPROM operation again to make further changes. Repeat steps.

Upon successful completion of the test the complete user program can be transferred from the RAM to the non-volatile EEPROM, using the following commands:

- PDDS command ”Save” (SAV) or
- PDDS commands ”Copy from RAM to EEPROM” (KOP) and ”Switch over from RAM to EEPROM” (UMS)

”Save” copies the lists and switches automatically to the EEPROM without impairing processing on the module and command output.

Following the switchover operation with the command UMS (from RAM to EEPROM and EEPROM to RAM) the user lists in the RAM and EEPROM are compared. Should any difference occur the controllers are switched to the ”manual” mode, the memories and timers are reset, and the commands present at the process interface are deactivated. The module transmits no send-location telegrams. The entries in the shared memory belonging to changed addresses of module inputs (EGn) are set to zero until new data are received for the first time after switchover. If the lists are identical processing will not be interrupted.

Simulation

The PDDS permits constant values to be specified to max. 32 individual module signals. These simulation data are stored on the EEPROM in the EEPROM mode and in the RAM in the RAM mode.

When the user lists are transferred from RAM to EEPROM and vice versa the simulation data are copied, too.

The simulation lists concerned are preserved in any changeover between RAM and EEPROM.

When the simulation process is cancelled via the PDDS the simulation data are erased from the active memory (EEPROM/RAM) and the module continues to operate with the data received via the bus or the generated values.

Command functions

Actuation from the control room

The module has no hard-wired control room interfaces. The module is actuated via the bus.

Actuation by higher-level automatic system

A higher-level automatic system actuates the module via the bus.

Protective commands

The logic operations for the protective commands are specified as required for the plant.

Release of drives

The output drive release AF for the power electronics is automatically set to ”1” when the module has finished initialization and the mode-dependent release is available from drive control ASP.

Checkback signals from the process and analog input

The drive-related checkback signals from the process can be connected to the hardware inputs of the module in case of the drive control functions (see function diagrams and connection diagrams).

The two analog inputs of a process interface are only intended for applications within the module itself and may only be connected to the appropriate inputs of the drive control function ASP.

Analog output

The position setpoints are output via the analog outputs AY1/Z11 and AY2/Z21. To adapt the position setpoint to the direction of action of the positioner it is possible to reverse this output in structuring..

Module configuration

Setting the operating mode

The operating mode (REG) and the cycle time of the module are defined in function block KON. This function block shall be at the top of the structure list, followed by the text elements TXT for function designations.

Operating mode	Module cycle time	KON input
Analog control	fixed: 100, 200 ms	REG, x x =100 msec x =200 msec

The module cycle time is determined by the number and the type of function blocks entered in the structure list. The cycle times indicated as "fixed" are minimum times. They apply if the times resulting from the structure list are shorter.

The time actually required is stored in register 205 and can be read from the PDDS.

The following functions can be implemented for each module:

- 2 ASP drive control functions

The module cycle time has to be taken into consideration.

The 2 process interfaces of the module are assigned to the ASP drive control functions.

The module is connected to the control room via the process operator station.

Setting the system hum filters

The system hum filter is defined in the KON function block, jointly for all analog inputs.

PDDS display	PDDS entry	Remarks
FIL	0	OFF
	or 16	16 2/3 Hz
	or 50	50 Hz (default setting)
	or 60	60 Hz

Setting the analog inputs and outputs

The configuration is defined in the KON function block. The first entry for an analog input or analog output is allocated to process interface 1 and the second entry is allocated to the process interface 2.

For example:

PDDS display	PDDS entry	Remarks
B01	= EIN, 0	Analog inp. 1 (VA1) E11 0 ... 20 mA
B02	= EIN, 4	Analog inp. 2 (VA2) E21 4 ... 20 mA
B03	= EIN, 4	Analog inp. 3 (VA3) E13 4 ... 20 mA
B04	= EIN, 0	Analog inp. 4 (VA4) E23 0 ... 20 mA
B05	= AUS, 4	Analog outp.1 (AA1) AY1 4 ... 20 mA
B06	= AUS, 0	Analog outp.2 (AA2) AY2 0 ... 20 mA

Setting the jumpers

Jumpers X200 ... X203 are used to set the type of analog value transmitter connected to the analog input.

When X20n is plugged in, the analog input is non-floating and can be used to connect 2-wire transducers supplied from the module.

When X20n is not plugged in, the analog input is floating and can be used to connect 2-wire transducers which are supplied from the module or are externally supplied.

n within 0 and 3.

Function blocks for analog control mode (REG)

In this operating mode, the function blocks are available for analog control tasks for single-variable and master control functions.

In this operating mode, no disturbance bits are sent for analog values, except at the output of the GRE function block.

The module cycle time can be specified in increments, as a fixed minimum time (cf. Entries into the KON configuration element).

The function blocks generally referred to above are given an index in the following list (if used here).

Function block	**Abbrev.**
BINARY FUNCTIONS	
Switch-off delay element	ASV
2-out-of-3 selection, binary	B23
Extended bit marshalling	BRA2
Dynamic OR gate	DOD
Switch-on delay element	ESV
Monostable flip-flop "break"	MOA
Monostable flip-flop "constant"	MOK
OR gate	ODR
RS flip-flop	RSR
AND gate	AND
Selector switch, 4-fold	WS41
DRIVE CONTROL	
Drive control function "Proportional output with extended capabilities"	ASP1
LIMIT SIGNAL ELEMENTS	
Limit signal for upper limit value	GOG
Limit signal generation	GRE
Limit signal for lower limit value	GUG

Function block	**Abbrev.**
ANALOG FUNCTIONS	
Absolute value generator	ABS
Limiter	BEG
Divider	DIV
Function generator	FKG
Integrator (with integrator stop)	INT1
Factor variation	KVA
Maximum value selector	MAX
Minimum value selector	MIN
Multiplier	MUL
Monitoring and select function	MVN
Differentiator	PDT
Delay element	PT0
Delay element	PT1
Square root extractor	RAD
Summing multiplier	SMU
Disturbance bit suppression	SZU
Time variation	TVA
Change-over switch	UMS
ANALOG CONTROL	
Auto/Manual station	HST1
PID controller (with integrator stop)	PID3
PI controller (with integrator stop)	PIR3
P controller	PRE
Setpoint integrator	SWI1
PUSHBUTTON SELECTION FUNCTIONS	
Pushbutton selection	TAW
Pushbutton selection with target value presetting	TAZ
ORGANIZATION FUNCTIONS	
Configuration element for operating mode setting	KON
Text element	TXT

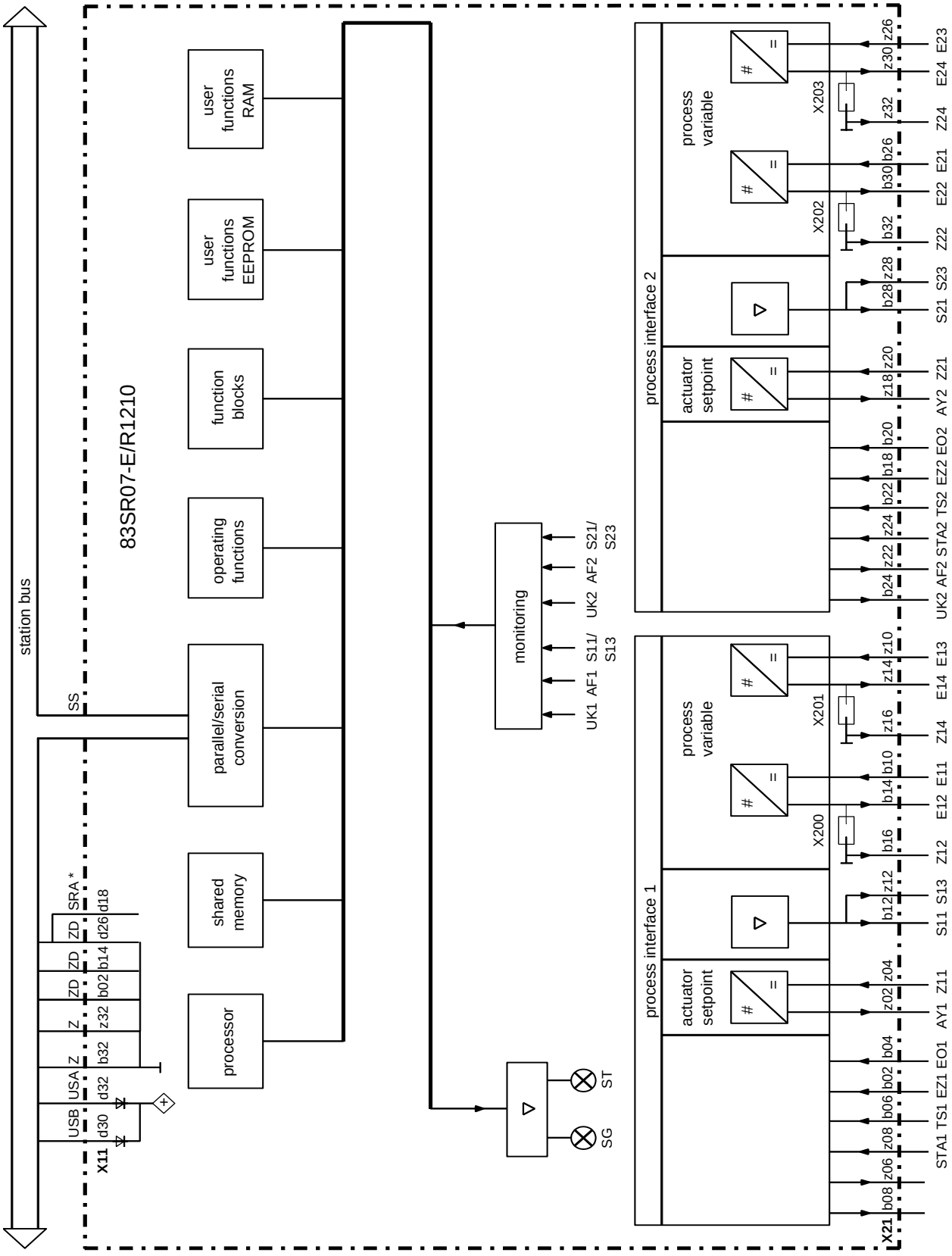
The detailed specifications of the function blocks as well as the procedure of structuring are described in the relevant function block descriptions.

Function diagram

Terminal designations:

The printed-circuit board is equipped with connectors X21 and X11.

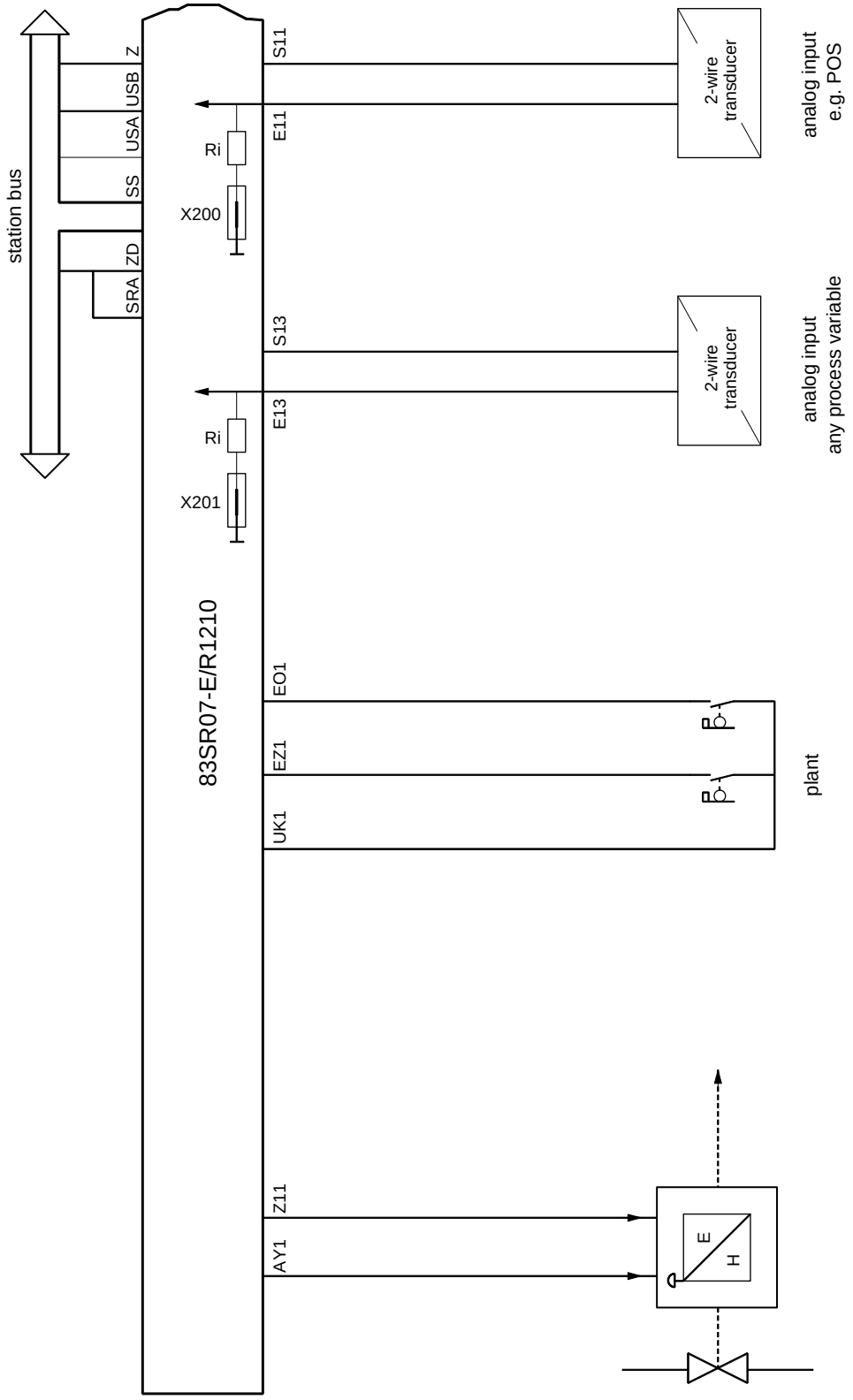
Connector X21 contains all the process inputs and outputs. Connector X11 contains the standard station bus interface and the operating voltages for the module.



* To ensure proper functioning of the module, terminal X11/d18 has to be connected with ZD (once per subrack).

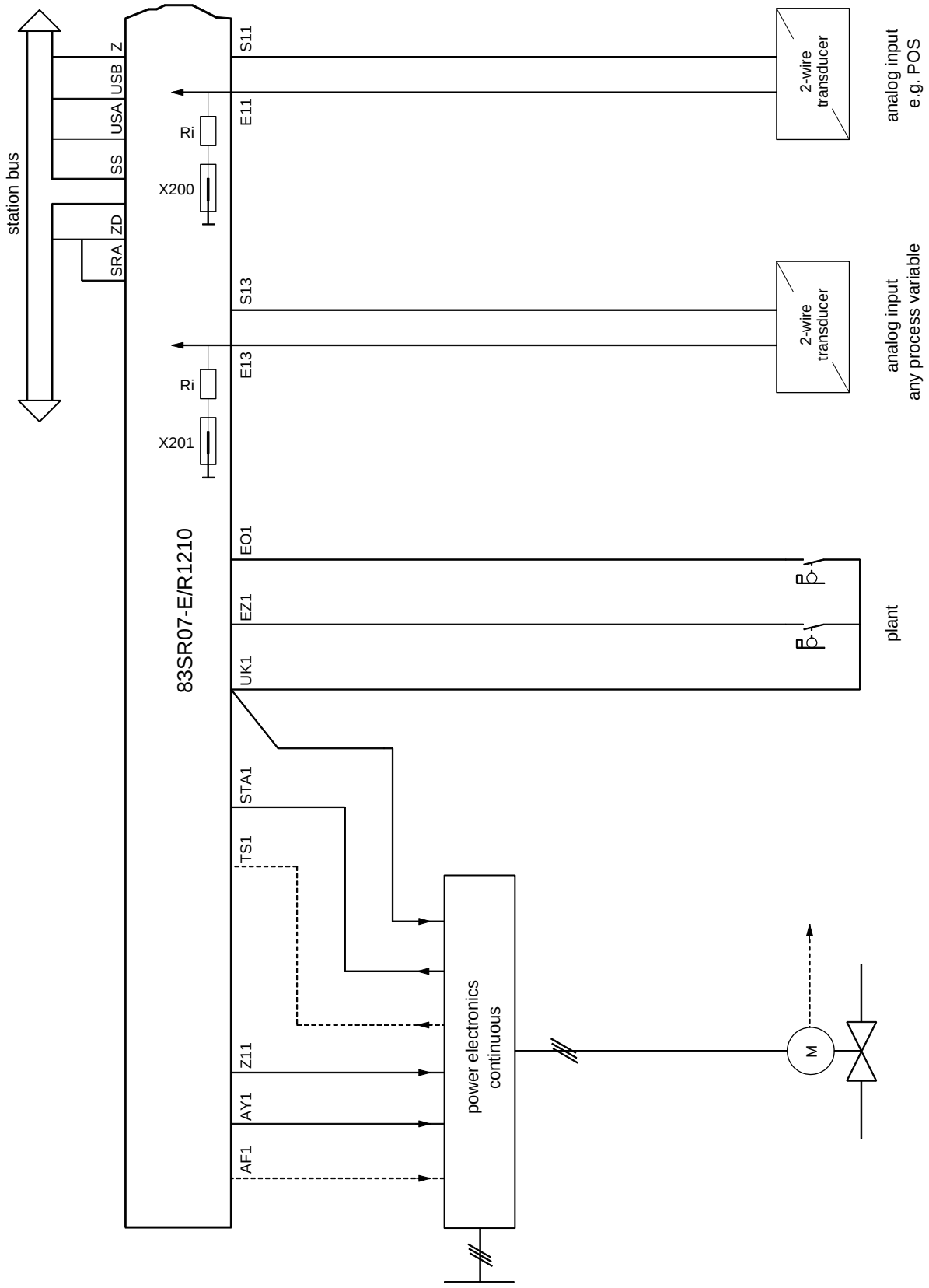
Connection diagram for an electrohydraulic or electropneumatic actuator (process interface 1)

2-wire transducer



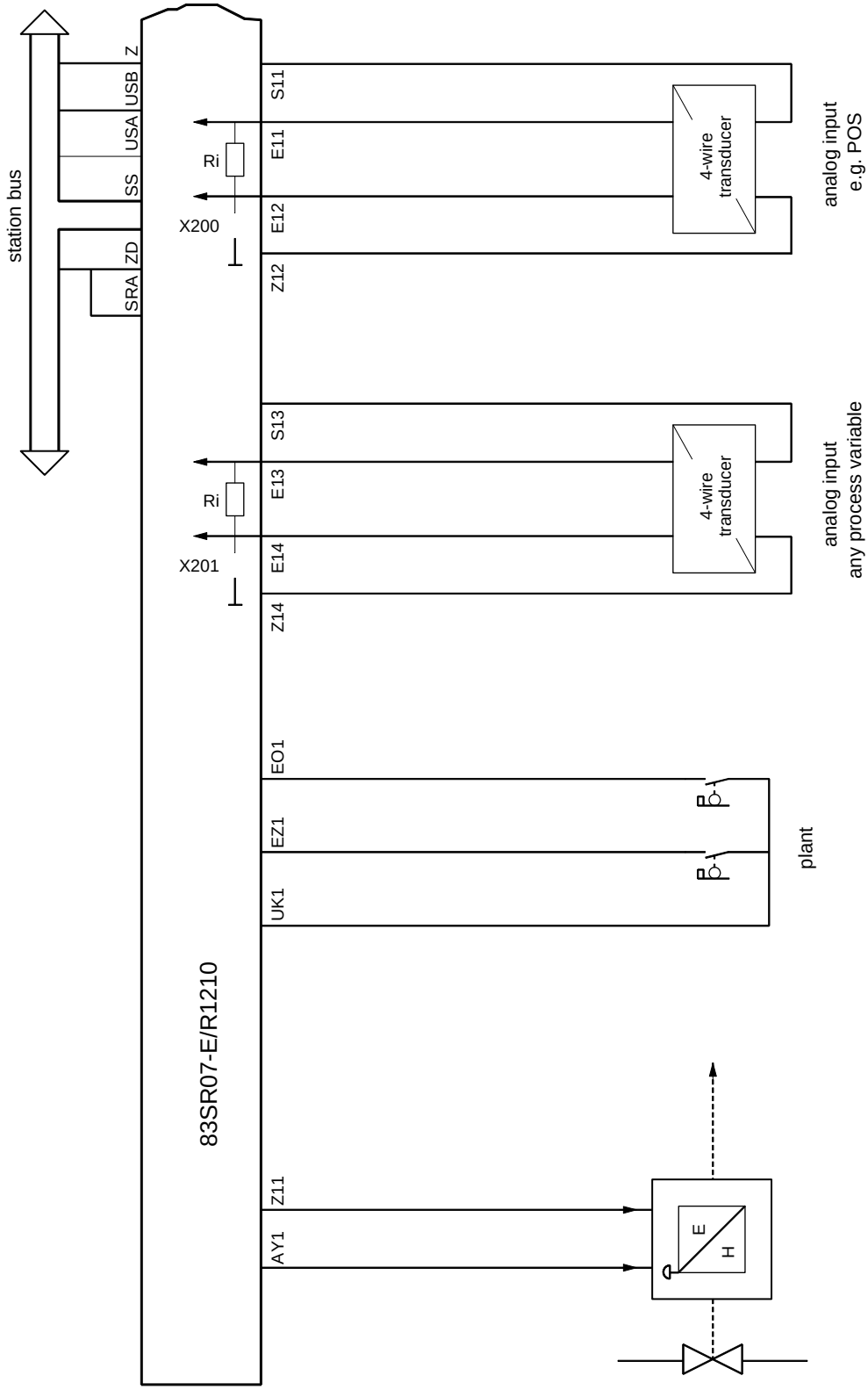
Connection diagram for an electric-motor-driven actuator (process interface 1)

2-wire transducer



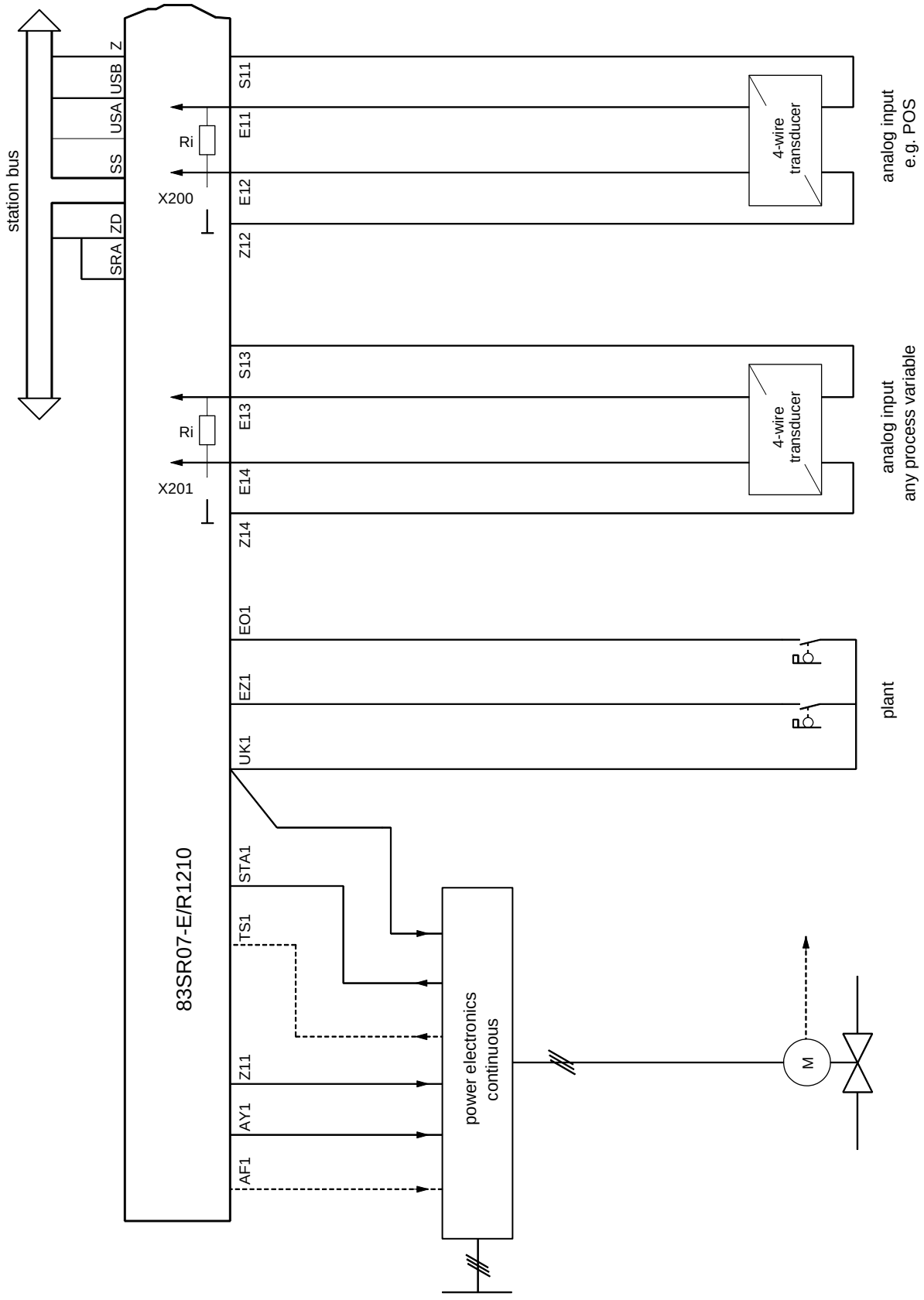
Connection diagram for an electrohydraulic or electropneumatic actuator (process interface 1)

4-wire transducer



Connection diagram electric-motor-driven actuator (process interface 1)

4-wire transducer



Mechanical design

Board size: 6 units, 1 division, 160 mm deep

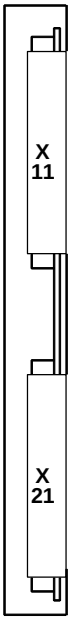
Connector: to DIN 41 612

1 x For station bus connection, 48-pin edge-connector, type F (connector X11)

1 x For process connection, 32-pin edge-connector, type F (connector X21)

Weight: approx. 0.55 kg

View of connector side:

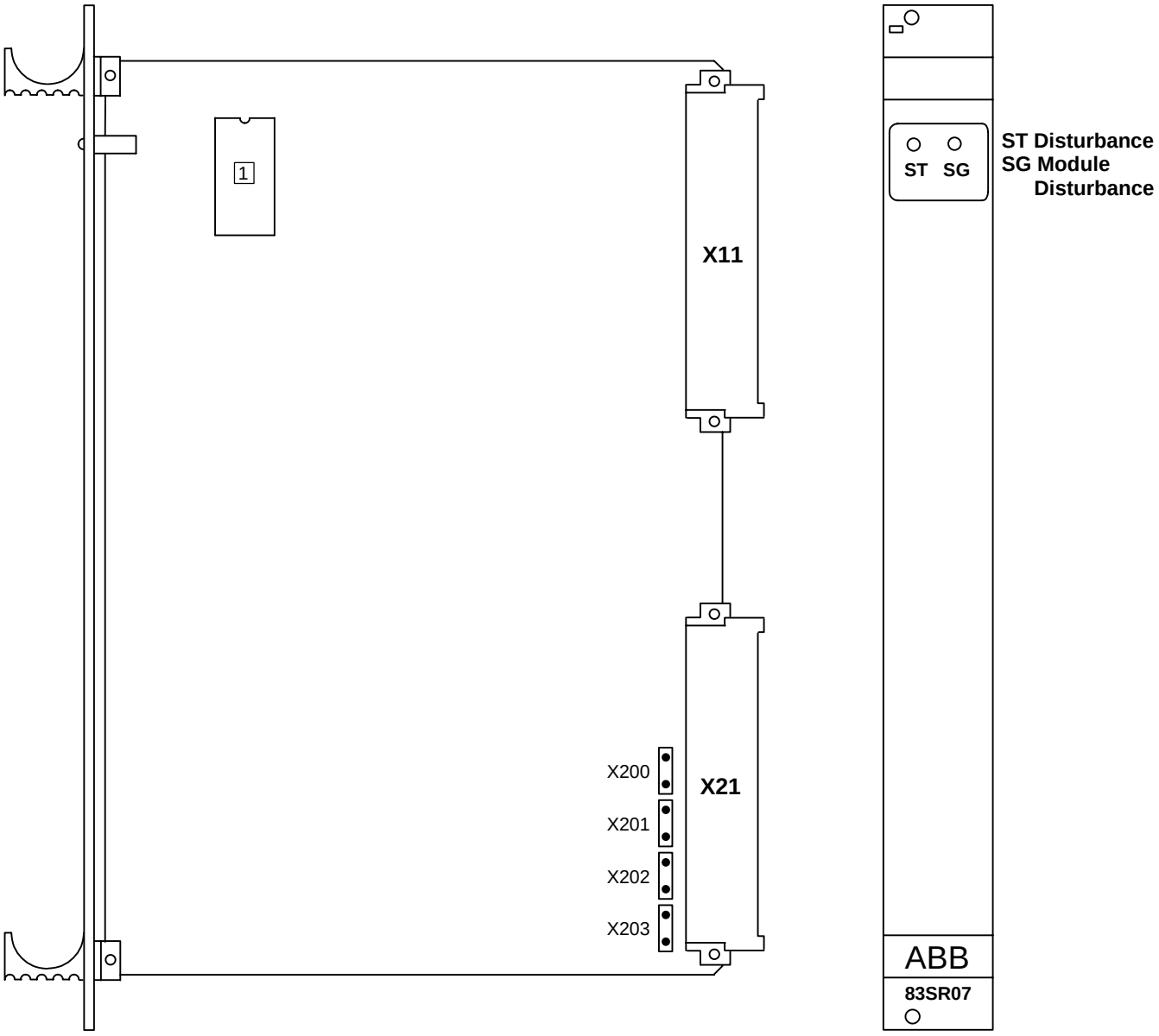


Contact assignments of the X21 process connector

View of contact side:

	b	*z*
02	EZ1	AY1
04	EO1	Z11
06	TS1	AF1
08	UK1	STA1
10	E11	E13
12	S11	S13
14	E12	E14
16	Z12	Z14
18	EZ2	AY2
20	EO2	Z21
22	TS2	AF2
24	UK2	STA2
26	E21	E23
28	S21	S23
30	E22	E24
32	Z22	Z24

Side view and view of the module front



1 EPROM programmed, order number: GJR2392741Pxxxx
xxxx = Position number according to the applicable program version.

Technical data

In addition to the system data, the following values apply:

Power supply

Operating voltage USA/USB	19.5 ... 30 V, typ. 24 V
Power consumption with USA/USB = 24 V	145 mA + output values
Power dissipation with USA/USB = 24 V	5 ... 8,4 W
	depending on operating voltage and configuration
Reference potential, process side	Z = 0 V
Reference potential, bus side	ZD = 0 V

BINARY SIGNALS

Input values

Direct connections for 2 process interfaces

EZx	Process checkback signal CLOSED	5 mA at 48 V
EOx	Process checkback signal OPEN	5 mA at 48 V
TSx	Local intervention	5 mA at 48 V
STAx	Disturbance in substation	5 mA at 48 V

x = 1, 2

Output values

Contact voltages, process side

for inputs EZx, EOx, TSx and STAx	UK1 = 48 V / ≤ 30 mA
	UK2 = 48 V / ≤ 30 mA

x = 1, 2

The outputs are short-circuit-proof, non-interfering and open-circuit-proof

Output values AFx

Drive release for power controller	US - max. 4 V
Output current	≤ 100 mA

x = 1, 2

The outputs are short-circuit-proof, non-interfering and open-circuit-proof

ANALOG SIGNALS

Input values Ex1 and Ex3

2-wire transducer

Jumpers X200, X201, X202 and X203 are plugged in.

Current ranges (corresponding to 0 ... 100 %)	0 ... 20 mA or
	4 ... 20 mA
Maximum value	-1 ... 50 mA
Input resistance Ri towards Z	50 ohms

x = 1, 2

Input values Ex1/Ex2 and Ex3/Ex4

4-wire transducers

Jumpers X200, X201, X202 and X203 are not plugged in.

Current ranges (corresponding to 0 ... 100 %)		0 ... 20 mA or 4 ... 20 mA
Maximum value		-1 ... 50 mA
Input resistance Ri towards Ex2 and Ex4		50 ohms

x = 1, 2

Accuracy of the input values

All data are based on 100 % of input value 20 mA

Accuracy:	in as-delivered condition (23°C)	≤ 0.1 %
	over a temperature range of 0 to 70 °C, aging, voltage range	≤ 0.3 %
Quantization error		≤ 0.02 %
Linearity error		≤ 0.1 %
Temperature sensitivity		≤ 50 ppm/K (typ. 30 ppm/K)
Errors due to digital linearization		1 LSB
Resolution:	at 0 ... 20 mA	12 bits
	at 4 ... 20 mA	12 bits
Common-mode rejection		120 dB
Normal-mode rejection at 16 2/3, 50 and 60 Hz		50 dB

Transducer power supply Sx1/Sx3

Output voltage	US - max. 4 V
Output current	≤ 50 mA

Outputs Sx1 are short-circuit-proof, non-interfering and open-circuit-proof.
Outputs Sx1 and Sx3 are interconnected internally.

x = 1, 2

Output values AYx/Zx1

Current ranges (corresponding to 0 ... 100 %)	0 ... 20 mA or 4 ... 20 mA
Burden	≤ 500 ohms

x = 1, 2

The outputs are short-circuit-proof, non-interfering and open-circuit-proof

Accuracy of the output values

All data are based on 100 % of the output value 20 mA

Accuracy:	in as-delivered condition (23°C)	≤ 0.1 %
	over temperature, aging, voltage range	≤ 0.4 %
Quantization error		≤ 0.02 %
Linearity error		≤ 0.1 %
Temperature sensitivity		≤ 50 ppm/K (typ. 30 ppm/K)
Resolution,	at 0 ... 20 mA	12 bits
	at 4 ... 20 mA	12 bits

Initialization time

Upon power connection or when the module is plugged in	2 ... 22 sec

Interference immunity (of the process inputs and outputs)

Electrostatic discharge immunity	DIN EN 61000-4-2	8 kV / 4 kV
Radiated, radio-frequency, electromagnetic field, immunity	DIN EN 61000-4-3	10V/m
Electrical fast transient/burst immunity	DIN EN 61000-4-4	2 kV
Surge Immunity	DIN EN 61000-4-5	2 kV / 1 kV
Conducted disturbances immunity	DIN EN 61000-4-6	10 V

ORDERING DATA

Order no. for complete module:
Type designation: 83SR07-E/R1210 Order number: GJR2392700R1210

Technical data are subject to change without notice!

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